46. The solar cell of claim **45**, wherein the anti-reflective coating layer comprises silicon nitride.

47. The solar cell of claim **36**, further comprising an anti-reflective coating layer disposed over the front surface of the semiconducting wafer.

48. The solar cell of claim **47**, wherein the anti-reflective coating layer comprises silicon nitride.

49. A method of fabricating a solar cell, the method comprising:

providing a semiconducting wafer having a front surface, a back surface, and a background doped region between the front surface and the back surface;

performing a set of ion implantations of dopant into the semiconducting wafer to form a back alternatingly-doped region extending from the back surface of the semiconducting wafer to a location between the back surface and the front surface, wherein the back doped region comprises laterally alternating first back doped regions and second back doped regions, and wherein the first back doped regions comprise a different charge type than the second back doped regions and the background doped region; and

disposing a back metal contact layer onto the back surface of the semiconducting wafer, wherein the back metal contact layer is aligned over the first and second back doped regions and is configured to conduct electrical charge from the first and second back doped regions.

50. The method of claim **49**, wherein the step of performing a set of ion implantations of dopant into the semiconducting wafer to form a back alternatingly-doped region comprises:

performing a blanket ion implantation of a first dopant into the semiconducting wafer, wherein the first dopant is implanted across the entire back surface of the semiconducting wafer; and

performing a masked ion implantation of a second dopant into the semiconducting wafer using a shadow mask disposed a predetermined distance away from the back surface of the semiconducting wafer, wherein the shadow mask comprises mask openings that are aligned with the locations on the semiconducting wafer where the second back doped regions are to be implanted.

51. The method of claim **49**, wherein the step of performing a set of ion implantations of dopant into the semiconducting wafer to form a back alternatingly-doped region comprises:

performing a first masked ion implantation of a first dopant into the semiconducting wafer using a shadow mask disposed a predetermined distance away from the back surface of the semiconducting wafer, wherein the shadow mask comprises mask openings that are aligned with the locations on the semiconducting wafer where the first back doped regions are to be implanted; and

performing a second masked ion implantation of a second dopant into the semiconducting wafer using a shadow mask disposed a predetermined distance away from the back surface of the semiconducting wafer, wherein the shadow mask comprises mask openings that are aligned with the locations on the semiconducting wafer where the second back doped regions are to be implanted.

52. The method of claim **49**, wherein:

the background doped region is n-type doped;

the first back doped regions are p-type doped; and

the second back doped regions are n-type doped.

53. The method of claim **52**, wherein the first back doped regions are doped with a dopant chosen from the group consisting of: boron, aluminum, and gallium.

54. The method of claim **52**, wherein the second back doped regions are doped with a dopant chosen from the group consisting of: phosphorous, arsenic, and antimony.

55. The method of claim **49**, wherein the semiconducting wafer is a silicon substrate.

56. The method of claim **49**, further comprising the step of performing an ion implantation of a dopant into the semiconducting wafer to form a front doped region extending from the front surface of the semiconducting wafer to a location between the front surface and the back surface, wherein the front doped region does not extend to or past the location of the back alternatingly-doped region.

57. The method of claim **56**, wherein the front doped region is p-type doped.

58. The method of claim **49**, further comprising the step of depositing an anti-reflective coating layer over the front surface and the back surface of the semiconducting wafer.

59. The method of claim **58**, wherein the anti-reflective coating layer is deposited using a Plasma-Enhanced Chemical Vapor Deposition (PECVD) process.

60. The method of claim **58**, wherein the anti-reflective coating layer comprises silicon nitride.

61. The method of claim **58**, wherein the step of disposing the back metal contact layer onto the back surface of the semiconducting wafer comprises:

ablating the anti-reflective coating layer to form separated openings in the anti-reflective coating layer over the first and second back doped regions; and

depositing metal contacts within the separated openings.

62. The method of claim **61**, wherein the step of disposing the back metal contact layer onto the back surface of the semiconducting wafer further comprises performing an electroplating process after the metal contacts have been deposited within the separated openings.

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